

# 力旺電子Briefing ■

**ememory**

# IPR Notice ■

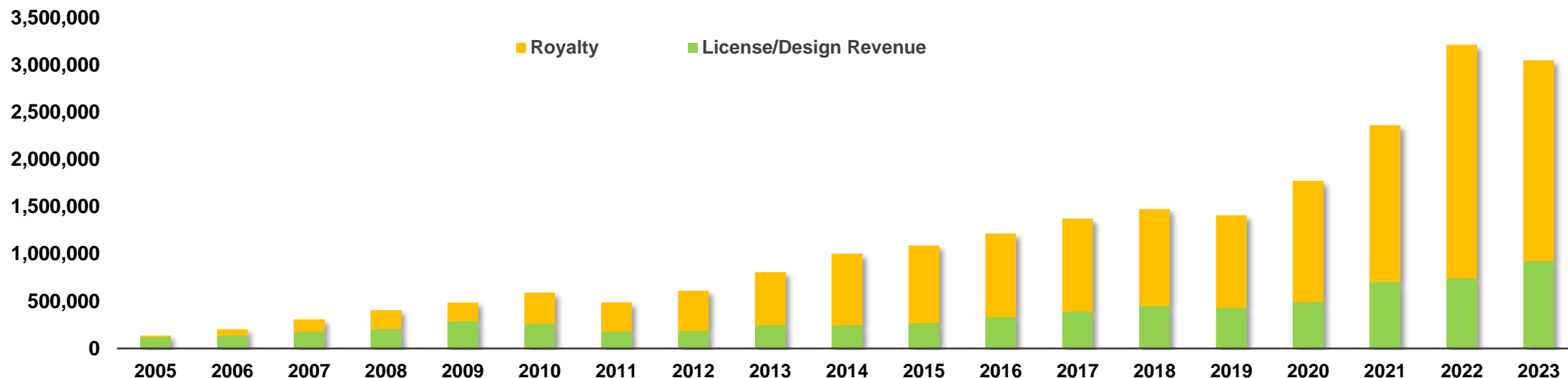
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# 公司介紹

- eMemory is the global leader of embedded non-volatile memory IP

## Revenue Trend

(Unit: NT\$ 1,000)



**Founded**  
In 2000

Based in Hsinchu, Taiwan.  
IPO in 2011. Over 60M wafers shipped.

**1200+**  
Patents Issued

193 pending patents. 357 employees with 68% R&D personnel.

**Best IP Partner**  
With TSMC

TSMC Best IP Partner Award since 2010.

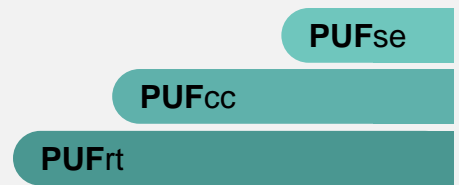
# 公司產品技術



With access to eMemory's widely verified IP process platform, PUFsecurity is uniquely positioned to provide **OTP and PUF-based** Security IP Solutions with **extensive availability** across various foundries and process nodes.

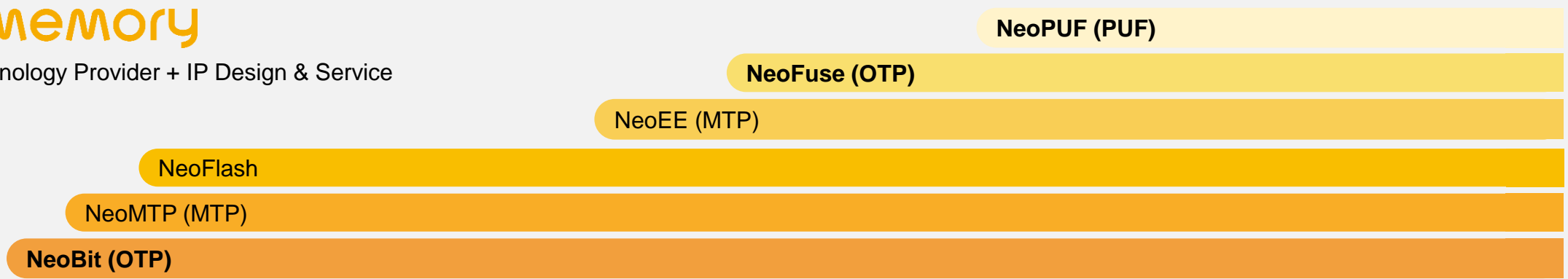
## PUFsecurity

PUF-based Security IP Design & Service



## eMemory

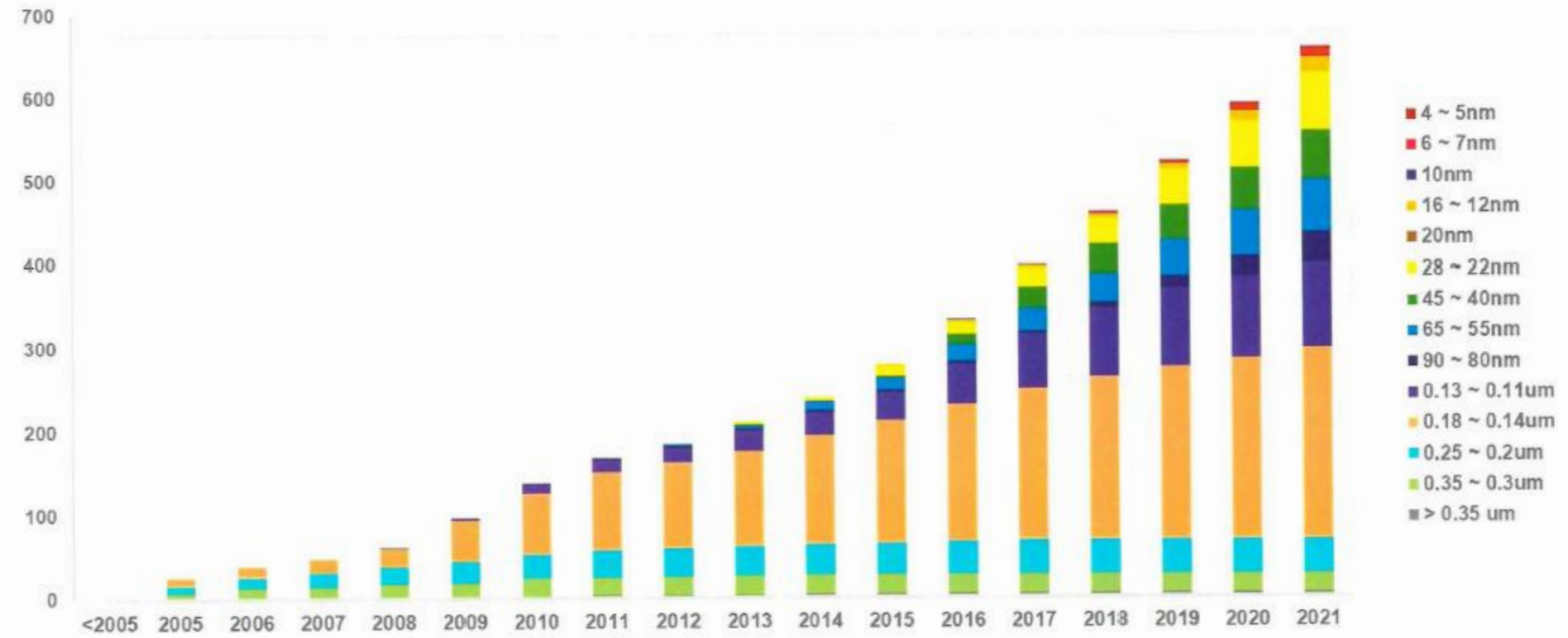
Technology Provider + IP Design & Service



# Registered IPs at TSMC



## Registered IP > 650

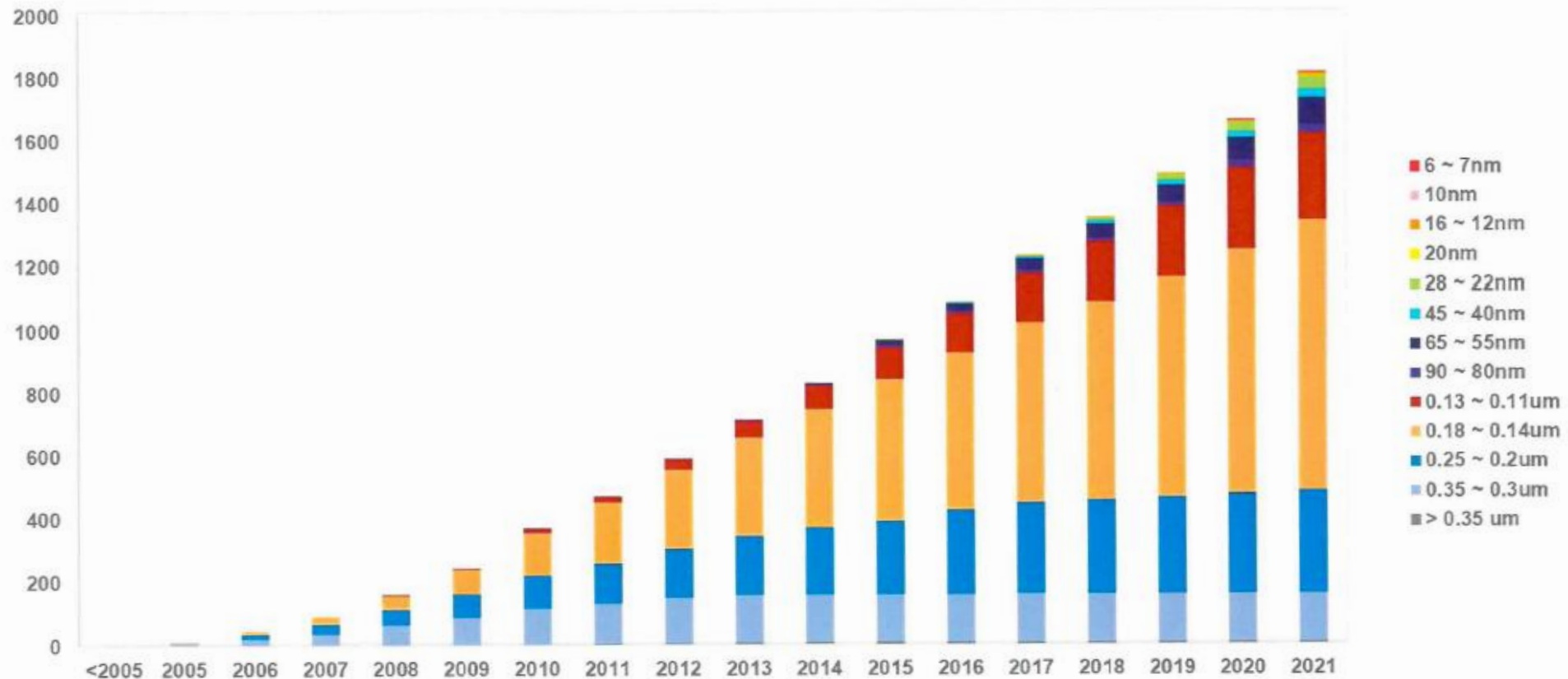


# NTOs at TSMC



Unleash Innov.

## New Tape Out Contribution > 1800

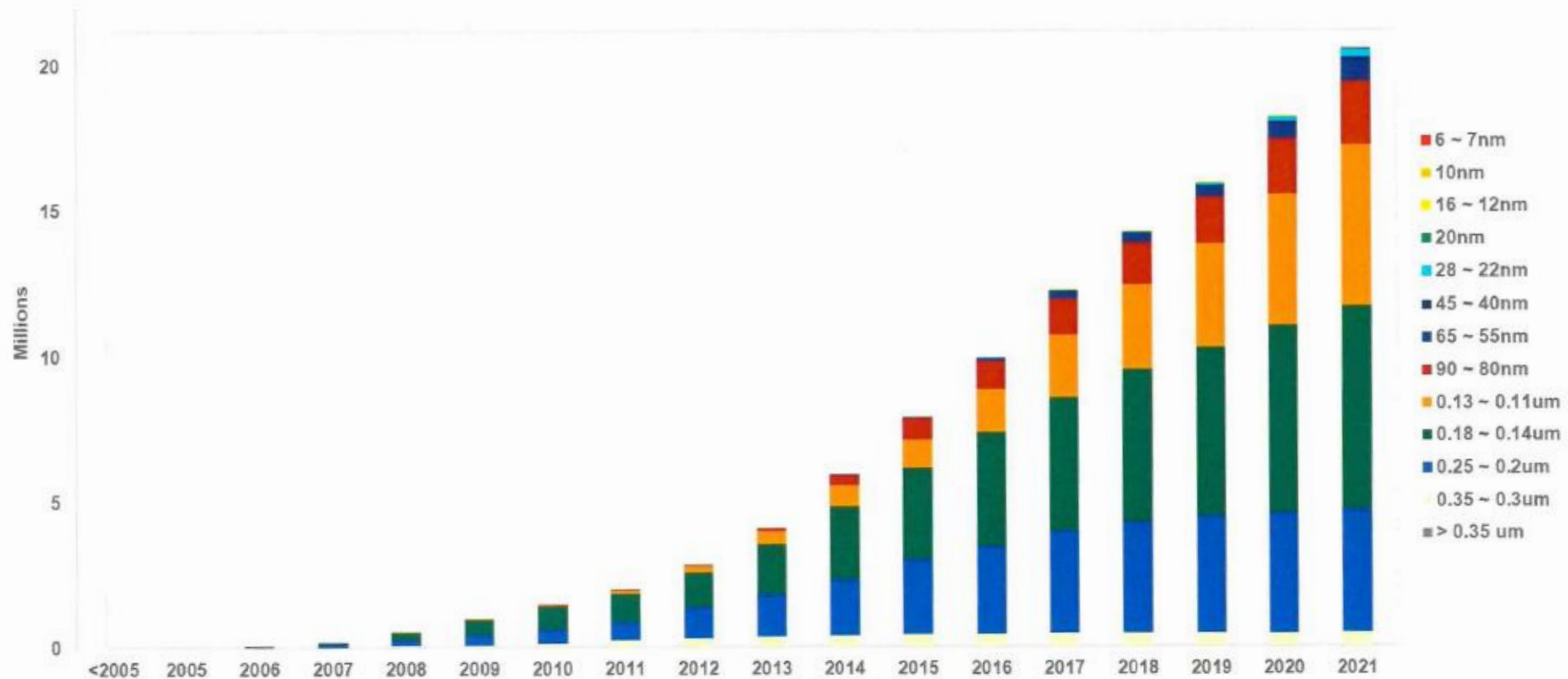


# Wafer Contribution at TSMC



Unleash Innovation

## Wafer Contribution > 20M



# Revenue and Tape-out by Technology

Year	NTO		Revenue (USD)		
	NeoBit	NeoFuse	NeoBit	NeoFuse	PUF-based
2002	3				
2003	29				
2004	40				
2005	68		\$ 4,217,380		
2006	133		\$ 6,202,270		
2007	220		\$ 9,402,479		
2008	253		\$ 12,896,211		
2009	268		\$ 11,695,587		
2010	284		\$ 15,873,331		
2011	254		\$ 15,399,098		
2012	270		\$ 19,620,768		
2013	363	1	\$ 25,436,669	\$ 382,084	
2014	371	3	\$ 31,831,985	\$ 328,787	
2015	311	11	\$ 30,943,426	\$ 1,080,373	
2016	270	28	\$ 30,247,340	\$ 3,636,142	
2017	257	61	\$ 34,619,653	\$ 5,238,351	
2018	253	86	\$ 31,834,860	\$ 10,773,223	\$ 85,000
2019	226	109	\$ 27,602,332	\$ 14,466,279	\$ 195,000
2020	248	182	\$ 30,378,346	\$ 26,437,660	\$ 434,998
2021	252	259	\$ 32,367,560	\$ 44,011,223	\$ 1,160,702
2022	264	231	\$ 35,327,060	\$ 63,762,480	\$ 4,207,209
2023	226	241	\$ 23,251,721	\$ 64,276,058	\$ 4,375,409
<b>Total</b>	<b>4,863</b>	<b>1,212</b>	<b>\$ 429,148,077</b>	<b>\$ 234,392,660</b>	<b>\$ 10,458,318</b>

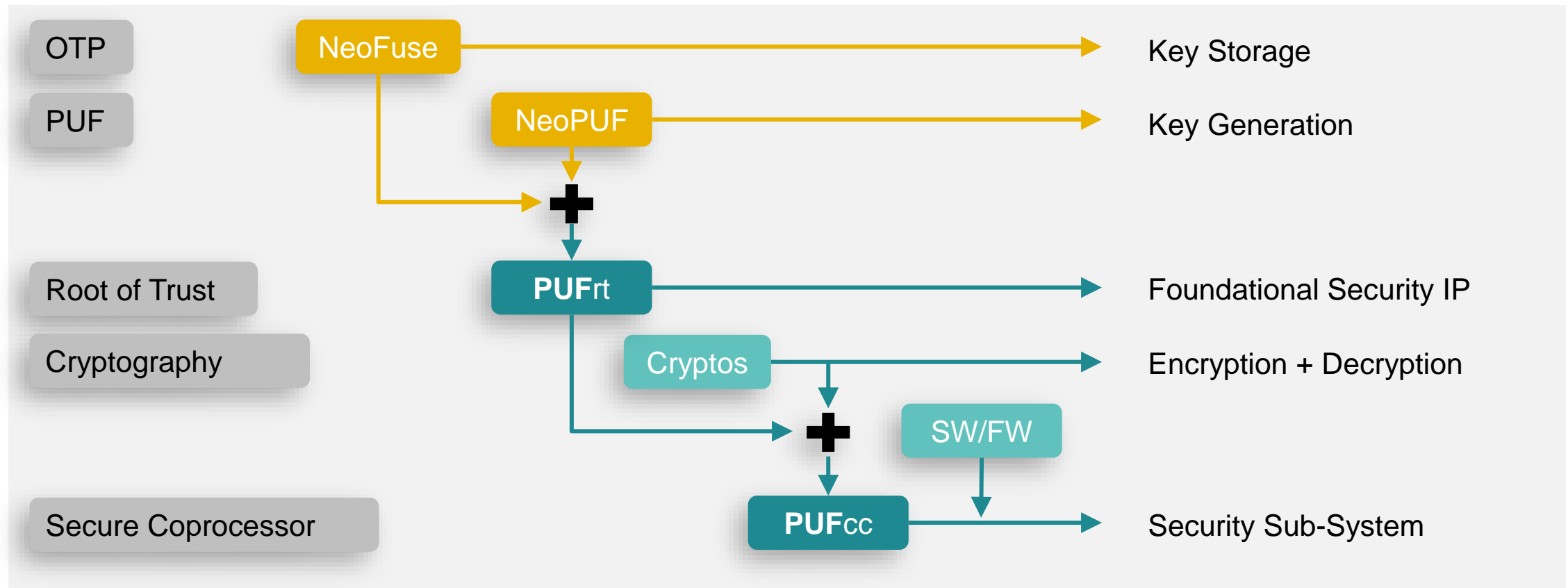
\*NTO stands for **New Tape-Out**

\* Revenue includes both **licensing** and **royalty**



# PUF-based Security Solutions

- Based on OTP Technologies, many different security functions IPs have evolved
- Regulations, such as TPM 2.0, now require Hardware Root of Trust



# Standards Drive Hardware-Based Security .



**Driving an open standard for silicon root of trust**



**Using asymmetric public/private key encryption technology and device ID to achieve fast and secure access to the network**



**Data Center**

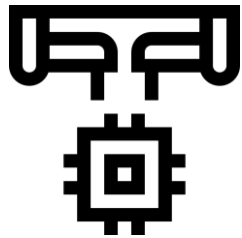


**IoT**

# Security Business Development

- As eMemory is an established IP company, there are different **platforms** that we can leverage for sales in security IPs and sub-systems

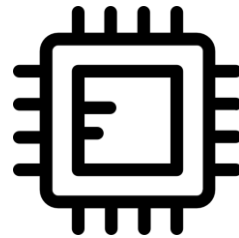
## Foundry Platforms



TSMC, Intel, UMC, GF, etc.

- Licensed our security technology to major foundries
- Co-promotional activities

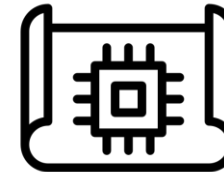
## CPU Partners



Arm, RISC-V, Cadence, etc.

- SoC customers looking for both CPU and security subsystems

## CSP



More to come

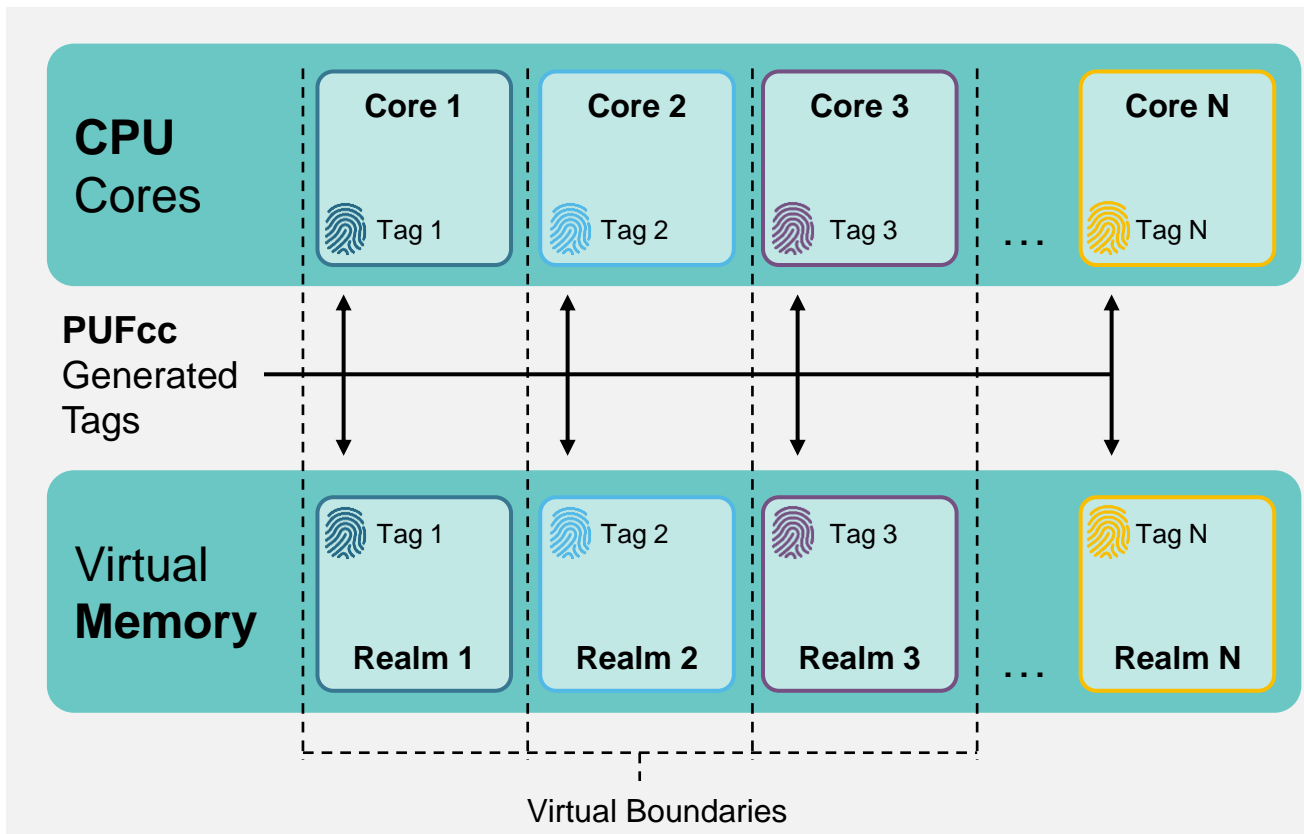
- Work with CSP and system companies for embedded security on a chip level

# Market Application ■

- Customers with many different applications will begin to adopt **PUF-based Security Solutions**

CPU	AI	SSD
DPU	DTV/STB	Wi-Fi
FPGA	ISP	And More.

# Next Computing: Confidential Computing

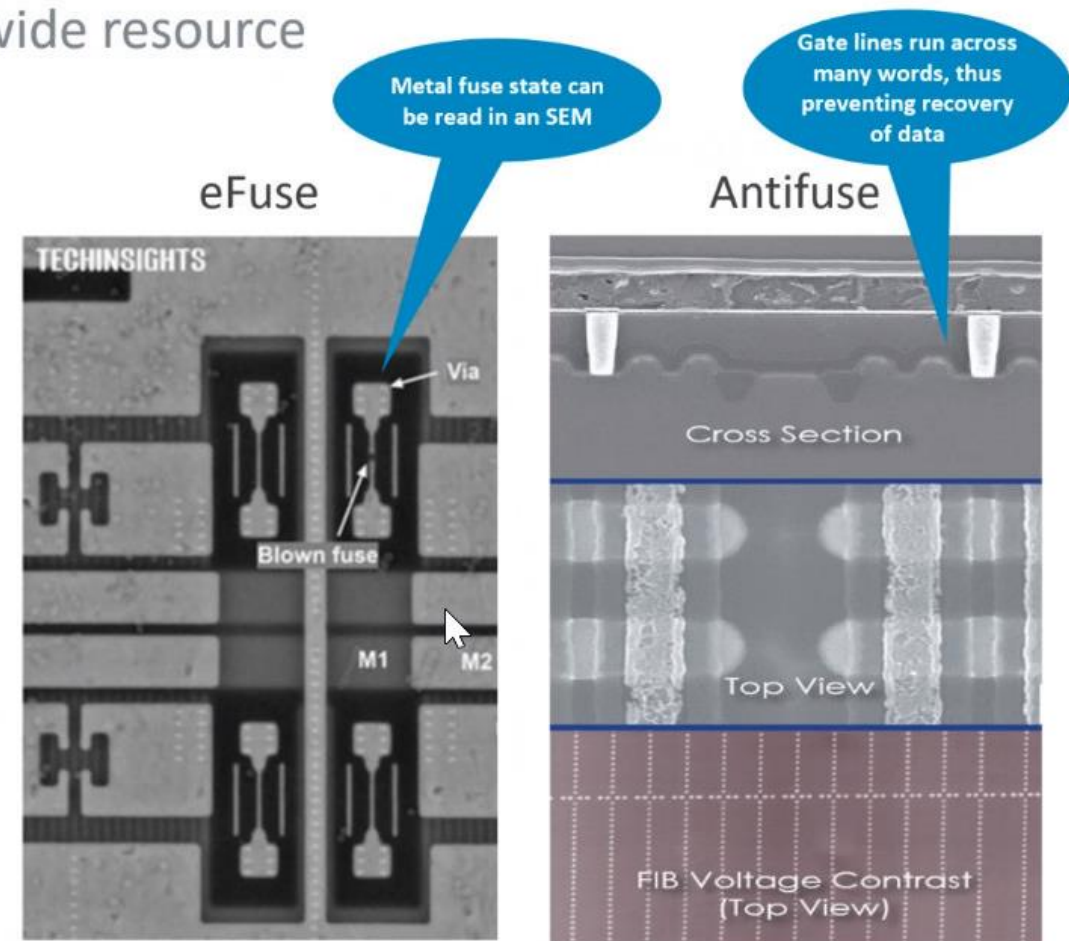


- **Protect data** in the Virtual Memory of Multi-Core CPUs
- CPU Cores and Virtual Memory have unique corresponding **tag numbers**
- Tag numbers are internally **randomly generated** by PUFcc (Crypto Coprocessor IP)

# AntiFuse OTP vs. eFuse

One Time Programmable (OTP) memory is a SoC-wide resource

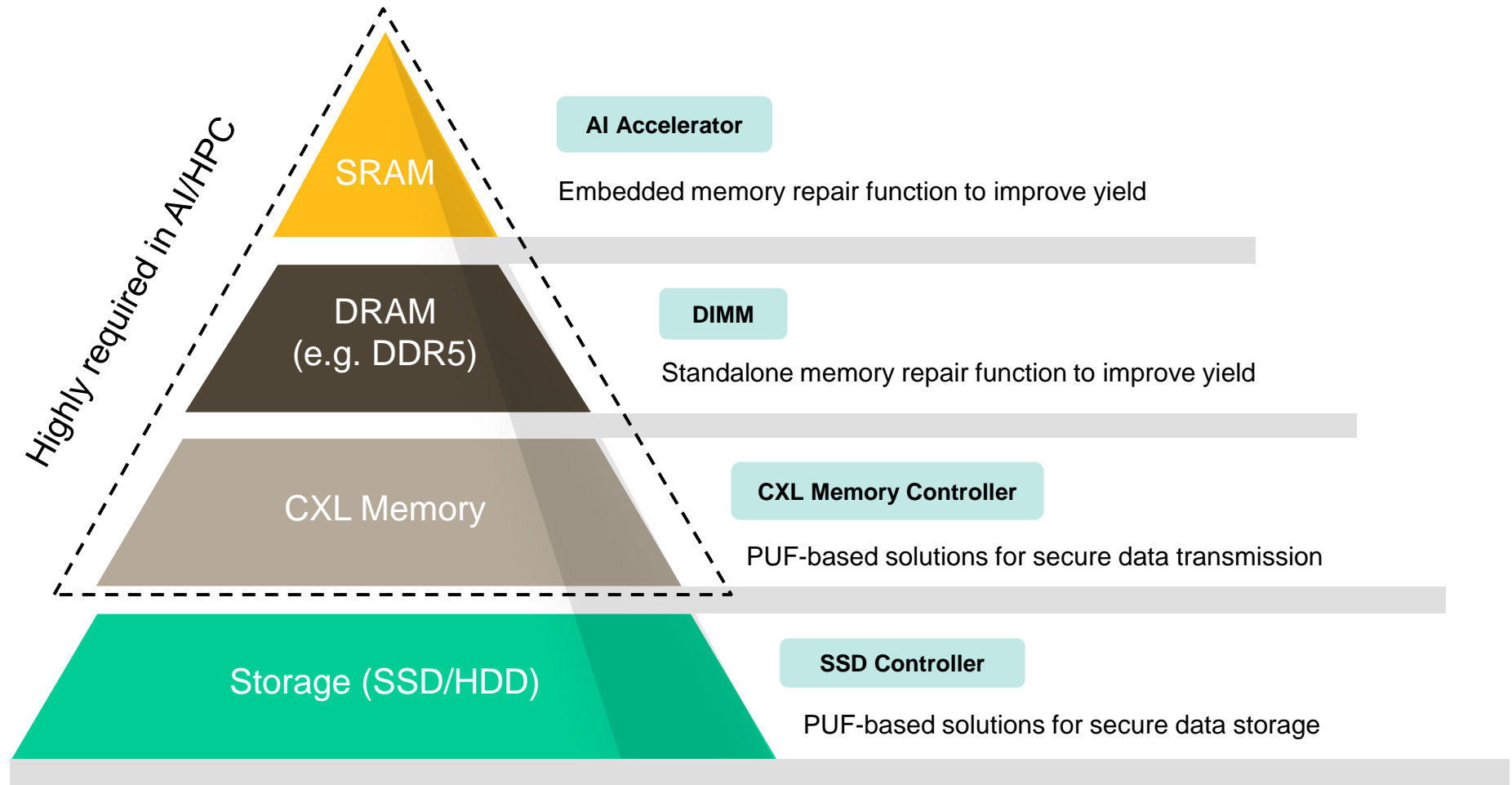
- RSS supports OTP as field-programmable to store confidential code and data
- eFuse:
  - Area efficient for smaller arrays
  - Typically not field programmable
  - Can be easily read by delayering SoC (a few \$k cost)
    - The secure channel key can be compromised
    - The device can then be cloned
- Antifuse OTP:
  - Cannot be read using a scanning electron microscope
  - Dense bit cells, efficient for large arrays
    - Macro periphery is large versus eFuse
  - Integrated charge pump enables field programming
  - PUF can be included for a small additional area
    - ~0.04mm<sup>2</sup> on 7nm for 128x32 bit PUF



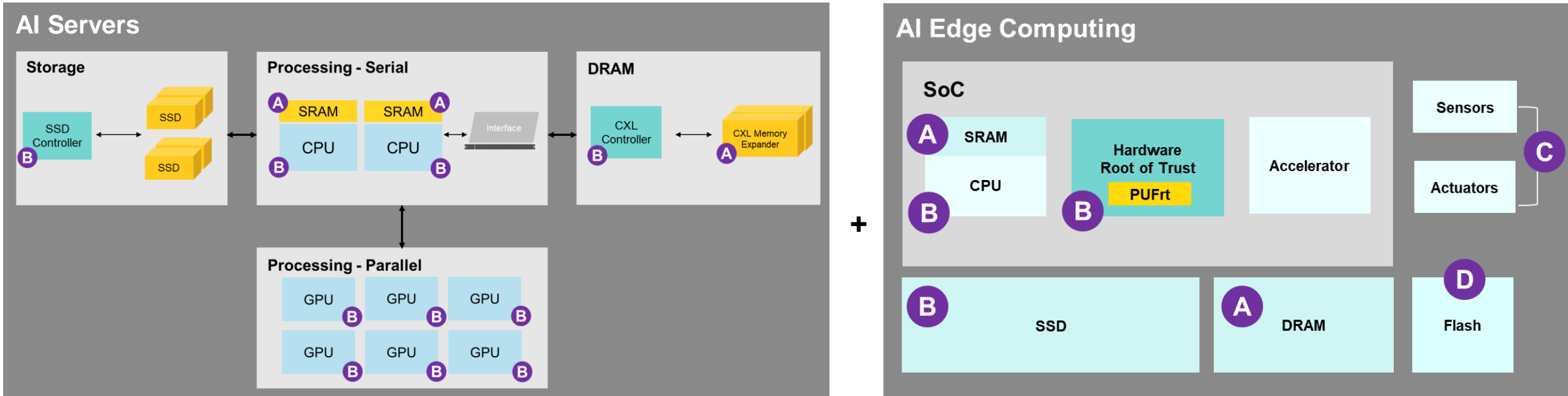
<https://semiengineering.com/the-benefits-of-antifuse-otp/>

# Example: eMemory Helps Memory.

- eMemory's security IP and OTP/MTP IP 1) ensure data security and 2) improve yield for SRAM and DRAM.



# eMemory for AI Servers and Edge Devices



**A Memory Repair**

**B Root of Trust provides:**

1. Key storage/generation
2. Cryptographic processing to protect AI models, input data and output results
3. Confidential Computing

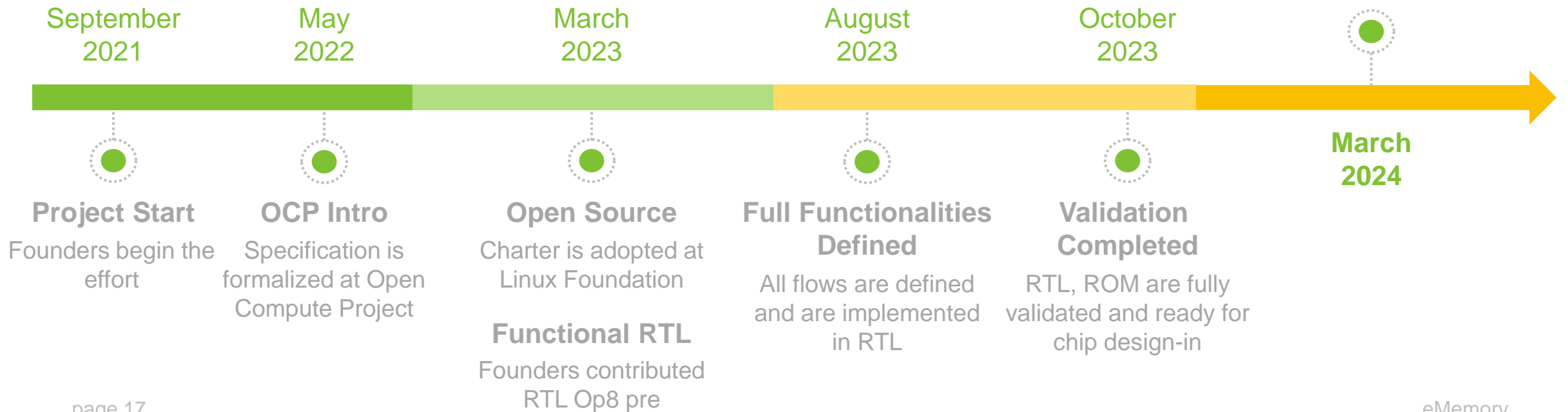
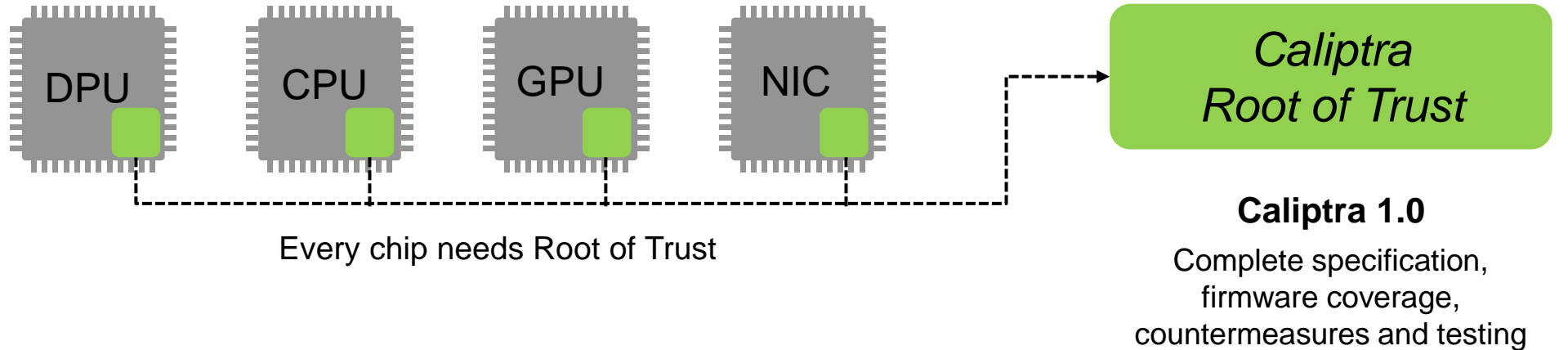
**C OTP needed for trimming analog circuits in Sensors and Actuators**

**D NeoFlash to replace conventional eFlash for a much lower cost**



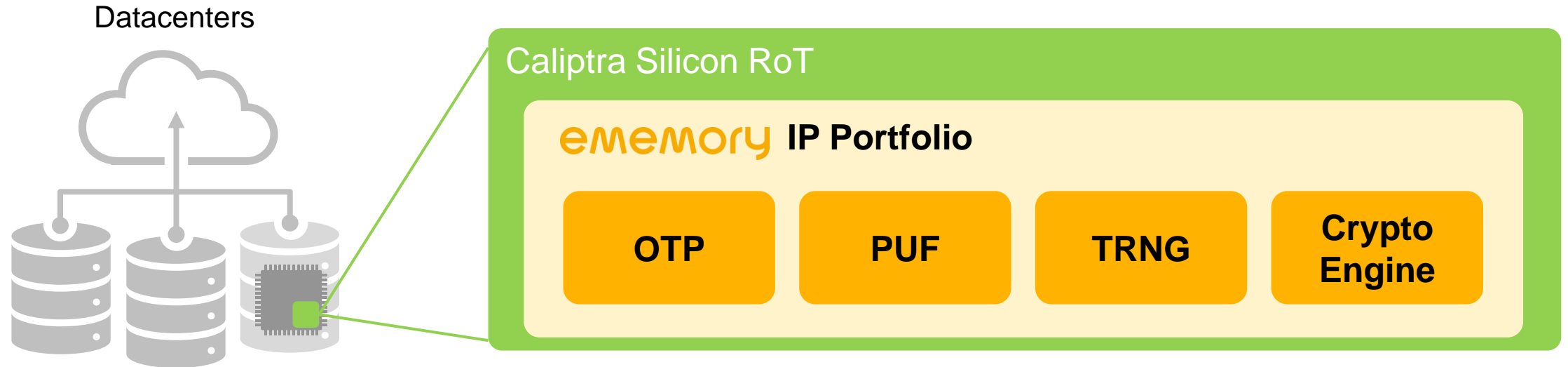
# Why is **Caliptra** so Important? ■

## Datacenter Chips



# What is the Important Role of eMemory in Caliptra?

- eMemory's root of trust IP is ready to meet Caliptra's requirements.



## Unique Chip Identity



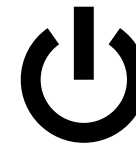
Chip Fingerprint

## Secure Attestation



Device Certificate

## Secure Boot

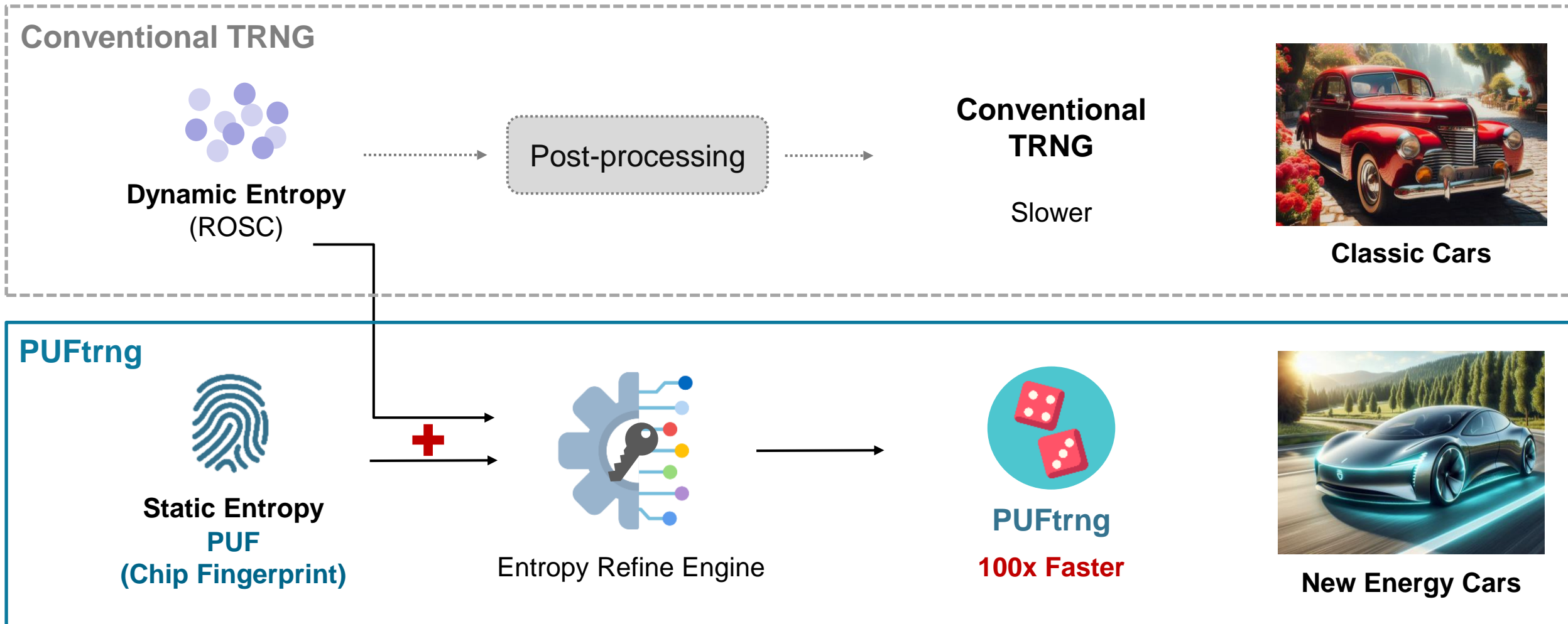


Boot into Trusted Operating System

# PUFtrng: 100 Times Faster than Conventional TRNG

- PUF-based conditioning algorithm provides high-throughput and high entropy quality

Similar to...



# Thank You for your time ■

For more information, please visit:

eMemory Website: <https://www.ememory.com.tw/>

PUFsecurity Website: <https://www.pufsecurity.com/>

The logo for eMemory, featuring the word "eMemory" in a white, lowercase, sans-serif font. The background of the slide is a blurred image of a circuit board with various components and traces.