eMemory 3Q24 Earnings Call Transcript

November 8th, 2024, 16:00-17:00 Taiwan Time

OPENING REMARKS

Dr. Charles Hsu, Chairman

Good afternoon, everyone. Thank you for attending our conference call today.

In October, we reached a significant milestone by successfully completing our first 3nm customer licensing project. The licensee, a global leader in CPU IP with applications in cloud data centers, has already begun collaboration with us on the CPU platform, marking a major step forward for us.

Our collaboration with Siemens on SRAM repair is also progressing well. Siemens' Tessent Memory Built-In Self-Test (BIST) tool holds a strong market share, and as AI chips require increasingly dense SRAM, managing yield in advanced processes is becoming more challenging. Traditional eFuse, typically suited for densities below 4kb, can no longer meet the density requirements for memory repair, and OTP density can be larger than several hundred kbits to a few megabits, which is needed for large density SRAM repair. Our partnership with Siemens will accelerate adoption among HPC customers seeking enhanced repair capabilities for SRAM.

As we mentioned previously, our technology development has advanced to 2nm, and chip design integration is underway at 3nm. With successful design wins at 5nm, 6nm, 7nm, 12nm, and 16nm entering mass production, along with the growing demand for security IPs in advanced processes, we see substantial growth potential ahead. We remain highly confident in our future.

Next, I'll invite our president, Michael Ho, to share our third-quarter performance and future outlook.

FINANCIAL RESULTS

Michael Ho, President

Q3 2024 Financial Results

Good afternoon, everyone. Now, let's begin with our 2024 third-quarter financial results.

The third-quarter revenue was eight hundred and ninety-nine million NT dollars (NT$ 899 mil), up 0.7% sequentially and up 14.3% year-over-year.

Operating expenses were three hundred and ninety-five million NT dollars (NT$ 395 mil), down 0.8% sequentially but up 6.7% year-over-year.

Operating income was five hundred and five million NT dollars (NT$ 505 mil), with an increase of 2% sequentially and an increase of 21% year-over-year.

Operating margin increased by 0.6 percentage point sequentially and increased by 3.1 percentage points year-over-year to 56.1%. Our net income, amounting to four hundred and fourteen million NT dollars (NT$414 mil), experienced a decrease of 12.9% sequentially but increased 2% year-over-year.

EPS for the quarter was 5.54 NT dollars (NT$ 5.54) and ROE was 54.6%.

Revenue across Different Streams

Next, let's move on to revenue contributions by licensing and royalty.

Licensing in the third-quarter accounted for 32.3% of the total revenue, down 3.0% sequentially and up 12.2% year-over-year.

Royalties in the third-quarter contributed 67.7% of the total revenue, increasing 2.6% sequentially and increasing 15.3% year-over-year.

Total revenue for the third-quarter increased by 0.7% compared to the previous quarter and increased by 14.3% compared to the previous year.

For the first three quarters of 2024, the licensing and royalty revenues are as follows:

Licensing in the first three quarters accounted for 31.5% of the total revenue, up 25.6% year-over-year.

Royalties in the first three quarters contributed 68.5% of the total revenue, increasing 18.5% year-over-year.

Total revenue for the first three quarters increased by 20.6% compared to the previous year.

Revenue by Technology

With that, I will comment on our revenue contribution by specific IPs.

NeoBit accounted for 31.2% of total licensing revenue in the third-quarter, increasing 23.2% sequentially and increasing 27.8% year-over-year. Its royalties accounted for 26% of total royalty, down 0.1% sequentially but up 35.5% year-over-year.

NeoFuse accounted for 30.9% of total licensing revenue in the third-quarter, down 10.1% sequentially and down 9.7% year-over-year. In terms of total royalty revenue, NeoFuse royalties increased by 4% sequentially and increased by 9.1% year-over-year, accounting for 71.5% of total royalties.

PUF-Based Security IPs contributed 12% of licensing revenue, decreasing 6.5% sequentially and decreasing 39% year-over-year, while its royalties accounted for less than 1% of total royalties.

MTP technology accounted for 25.9% of total licensing revenue, down 15.3% sequentially but up 139.5% year-over-year. Royalty from MTP decreased 7% sequentially but increased 25% year-over-year, accounting for 2.5% of total royalties.

For the first three quarters of 2024, the revenues by technology are as follows:

NeoBit licensing revenue increased 36.3% year-over-year and royalty increased 11%, accounting for 25.8% of the total revenue.

NeoFuse licensing revenue increased 9.2% and royalty increased 20.4% year-over-year, contributing to 61% of the total revenue.

PUF-based security IP licensing revenue decreased 10.6% year-over-year, while the royalty contribution was less than 1%, accounting for 3.5% of the total revenue. We expect PUF-based revenue to significantly increase in Q4.

MTP technology licensing revenue increased 85.5% year-over-year and royalty revenue increased 55%, accounting for 9.7% of total revenue.

Royalty Revenue by Wafer Size

Now, let's look at royalties for 8-inch and 12-inch wafers.

8-inch wafers accounted for 40.9% of royalties, down 1.2% sequentially but up 30% year-over-year.

12-inch wafers contributed 59.1% of royalties, increasing 5.5% sequentially and up 7% year-over-year.

In total, 179 product tape outs were completed in the third-quarter. We will provide more information in the management report.

FUTURE OUTLOOK

Michael Ho, President

In the next section, I will address our future outlook.

For licensing revenues: Licensing revenue will continue its growth momentum due to strong demands from both foundries and chip companies.

For royalty revenues: We expect royalty will continue its growth momentum as accumulated tape outs in 16/12/7/6nm enter the production stage, along with continued market share gains in mature applications.

Moving on to new IP technology and business development.

New IP Technologies:

1. NeoFuse/NeoPUF were successfully verified in the N3P process, with design in and evaluation cases ongoing.
2. NeoMTP for 4-color ESL/e-Paper display driver has been successfully verified in customer products and will soon ramp up.
3. We are developing 2nm technologies with leading foundries.

Business Development Platform:

1. The CPU architecture for security IP is expected to start contributing to revenue.
2. eMemory and Siemens are offering a groundbreaking SRAM repair toolset that integrates Siemens' Tessent MemoryBIST software with eMemory's NeoFuse OTP.
3. PUFsecurity is collaborating with Arm on PSA Certified RoT Component Level 3 Certification for its Crypto Coprocessor, providing a robust security subsystem essential for the AIoT era.

This concludes my comments. Next, I will pass the time to Charles.

CHAIRMAN REMARKS

Dr. Charles Hsu, Chairman

(Page 13: eMemory Enables HPC in AI Applications)

High-density SRAM plays a critical role in AI accelerators. However, increasing SRAM density brings yield challenges. Today, we'll explore how eMemory's NeoFuse OTP, integrated with Siemens' Tessent tools, provides a high-yielding, cost-effective solution to repair SRAM memory.

(Page 14: Why is High-Density SRAM needed in AI?)

In AI applications, the AI accelerator plays a crucial role in enabling faster model training, quicker predictions, and more efficient application performance. High-density SRAM is particularly important in AI accelerators to help them work faster and use less power, especially in three key areas: buffer memory, AI model training, and Computing in Memory (CIM) for inference.

In buffer memory, which is a high-speed storage between the different processing stages, high-density SRAM acts as a holding space for data in AI accelerators to ensure that everything runs smoothly. It functions like a large, fast-flowing funnel, temporarily storing and quickly passing data to different parts of the accelerator. With high-density SRAM, the buffer memory can handle large amounts of data without slowing down, while maintaining efficiency in power and speed during data transfers.

During AI model training, where substantial data processing is required as the model learns, high-density SRAM serves as a large and fast workspace. This allows the AI accelerator to access data quickly to speed up training and handling multiple data in parallel without compromising training time. Furthermore, the high density of SRAM provides enough on-chip storage to store large datasets directly, minimizing the need for slower external memory.

Lastly, in Computing in Memory for Inference, where the AI model generates predictions, high-density SRAM allows the AI accelerator to do quick calculations directly within the memory, instead of moving data to separate processors. With everything happening in one place, the AI model can make predictions quickly, which is important for tasks that need real-time responses, such as voice recognition. Furthermore, by reducing data movement, high-density SRAM also enhances power efficiency.

(Page 15: eMemory enables High-Yielding SRAM)

As I discussed in my talk last year, increasing the density of SRAM memory leads to a decrease in yield as the technology scales to smaller dimensions. However, eMemory's OTP can help repair defects in SRAM memory, enabling higher yields.

To refresh your memory, SRAM repair involves storing the locations of defective memory cells on OTP, enabling redundant memory cells already present in SRAM to replace the faulty ones. NeoFuse OTP is ideal for this purpose due to its smaller cell size compared to eFuse, making it particularly advantageous for high-density SRAM repair, where higher-density OTP is needed. Additionally, NeoFuse OTP is flexible enough to support various memory form factors, such as 3D or multi-chip packages, and ensures higher yield during production.

(Page 16: Partnering for Success: eMemory and Siemens)

eMemory provides OTP with an interface for Siemens MBIST (Memory Built-in Self-Test). By integrating eMemory's OTP technology with Siemens' Tessent Tool, we achieve more efficient SRAM repairs than conventional methods.

To achieve optimal SRAM repair, the Tessent memory Built-In Self-Test (BIST) controller is used to test the memory. After testing, the Built-In Redundancy Analysis (BIRA) module analyzes the defective bits and calculates the necessary repair

information. This information is then transferred to the SRAM repair ports and Built-In Self-Repair (BISR) registers. The repair information is then sent to the Tessent Memory BISR controllers, where it is written onto eMemory's NeoFuse OTP through our interface.

During device power-up, the Tessent tool reads the repair data from OTP and loads it into the BISR registers. This process instructs the SRAM controller to replace the defective bad bits with redundant bits already in the SRAM.

By combining eMemory's OTP with Siemen's Tessent Tool, we can achieve higher repair density and flexibility across any form factor of SRAM using a pre-integrated and verified solution that is simple to adopt. This not only reduces integration costs, but also minimizes costs associated with yield loss.

(Page 17: On-System Repair for AI Accelerators)

The Memory Built-in Self-Test (MBIST) tool is groundbreaking in its ability to quickly repair AI accelerators even after they have been integrated onto the system. Initially, memory testing, analysis, and repair relied on manual processes and specialized equipment, which had to be completed during the testing phase. This meant that once systems were deployed in-field, such as in expensive AI servers, automotive, and more, memory repairs could not be performed after leaving the testing phase.

With MBIST and Memory Built-in Self-Repair (MBISR), on-system repair becomes possible. By automating testing, analysis, and repair, MBIST not only saves time, costs, and resources, but also overcomes the bandwidth limitations of external memory testing tools. More importantly, on-system repair techniques can be applied to multiple chip stacks like chiplet architecture or after system packaging, which ensures reliability and functionality post-packaging. Chiplets typically contain large amounts of SRAM required for processing, which means high-density OTP is needed for effective repair. This approach is very suited for AI accelerators, which often have more complex designs and require faster, more efficient repairs.

(Page 18: eMemory enables HPC in AI Applications)

In addition to SRAM repairs, eMemory's integrated OTP IP is also needed for:

1. Replacing ROM to store Boot Codes when the AI system is booted up.
2. Storing the secret key and unique ID which are required in AI system to protect training data, AI models, and output data.

Therefore, eMemory's OTPs can enable AI by supporting high-speed SRAM repair, as well as storing boot codes, root key and unique ID for the root of trust in security functions.

With AI booming, we foresee continuous business growth over a long period.

That concludes my remarks. Thank you very much for your time.

Next, we will enter the Q&A session.

CLOSING REMARKS

Dr. Charles Hsu, Chairman

For more information about our PUF-based security IPs and technology, we encourage you to visit our PUFsecurity website at https://www.pufsecurity.com/ and check out our articles and other materials.

Thank you once again for your patience and support for eMemory. We will continue to work hard on technology and IP innovation and PUF-based hardware security solutions for our customers and bring higher returns for our shareholders. Thank you!