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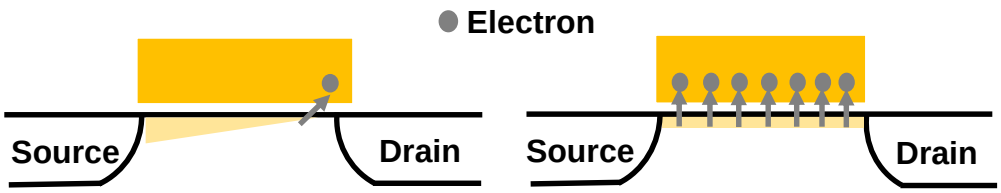
Optimum Selection of MTP Solutions for Product Design

WHITEPAPER

Introduction – A high degree of chip integration in System-On-Chip design (such as microprocessor control units, touch panel controllers, LCD drivers, wearable devices, type-C solutions**,** and Internet of Things systems) makes embedded nonvolatile memory (e-NVM) indispensable. e-NVM solutions can be divided into two types. The first is compact and fabricated through a more complicated manufacturing process than foundries usually offer because it requires more masking layers and process steps. The second, called "logic e-NVM", can be fabricated by using a CMOS logic process both to eliminate design barriers and lower manufacturing costs. The text below focuses on a comparison of different types of programming/erasure schemes in logic e-NVM solutions.

Programming Schemes – Logic e-NVM is usually a single poly NVM solution where the poly gate is used as a floating gate to store electrons and which is compatible with basic logic circuit fabrication processes. Channel Hot Electron (CHE) injection and *Fowler–Nordheim (*FN) tunneling are the main programming methods for injecting electrons to the floating gate for data storage. Although FN tunneling can be carried out at low power in order to support cluster programming, complete programming would take longer time because of the slow programming speed. Concerns about coupling ratios mean it would also need large cell size, and a more complicated peripheral circuit would be required to support the necessary high programming electrical field. A specialized array scheme and circuit design would be needed to overcome these drawbacks, but the side effects would still become insurmountable as demand for memory density increased.

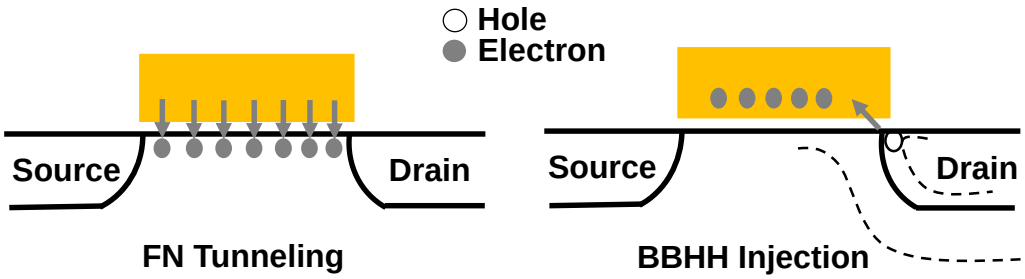
With CHE injection, programming time is about 1/1000 that of FN tunneling, and ***medium-high*** programming voltage is needed; thus, memory cell size can be smaller and the peripheral circuit for managing high voltages can also be simpler. The programming current for CHE injection is higher than FN tunneling but remains within acceptable limits for commercial applications. Considering testing times and e-NVM IP area, the kind of e-NVM solutions programmed by FN tunneling may be limited to applications that require low density. Since applications requiring medium to high density e-NVM are still the mainstream, e-NVM solutions programmed by CHE injection can be widely used.



Channel Hot Electron Injection **FN Tunneling**

Erasure Schemes – While programming involves injecting electrons to the floating gate, erasure means eliminating or emptying electrons from the floating gate. This can be achieved by pulling out electrons or by neutralization. As mentioned above, FN tunneling is not appropriate for e-NVM with medium to high density owing to its extremely slow programming speeds. However, such low speeds may have a limited effect on erasure and may therefore be acceptable in this context. Almost all e-NVM solutions offer chip or sector erasure; in other words, density of at least several kilo-bits are erased at one go in order to keep the whole-chip erasure time within acceptable limits. Thus, FN tunneling is often used for erasure schemes in e-NVM solutions.

Band-to-Band Hot Hole (BBHH) injection is another scheme used for erasure operations. With BBHH injection, holes with positive charges are pulled into the floating gate to neutralize the electrons with negative electrons and eliminate them from the floating gate. However, BBHH injection leads to oxide hole trapping, and the Band-to-Band tunneling effect means trapped holes will cause immediate and significant gate oxide damage. Oxide degradation leads to shrinkage of the sensing window after programming/erasure cycling, which leads to reduced reliability and endurance. Clearly, this impairs the performance of e-NVM solutions.



Comprehensive Comparison – In this section, we shall give a comprehensive comparison of different combinations of programming and erasure types. Power consumption, total testing time (especially programming/erasure time), area, and reliability are the main factors to be considered when selecting logic e-NVM solutions. As the table below shows, e-NVM solutions using FN tunneling for programming and erasure are completely unsuitable for medium to high density applications owing to concerns about area and testing costs. On the other hand, such solutions are a good choice for applications requiring low density and low power consumption, such as RFID and PMIC, since the effect for total testing time and area usually fall within acceptable limits. But programming by CHE injection is the clear choice for e-NVM markets needing medium to high density (i.e. most markets).

By contrast, total erasure time is often not as critical, since chip or sector erasure is universal and so there is minimal impact on total operation/testing time. Nevertheless, the effect of erasure on oxide degradation has to be considered, as logic e-NVM solutions must be able to endure from several hundred to several thousand programming–erasure cycles. If erasure operations cause oxide degradation—for example, through BBHH injection inducing hole trapping in gate oxide—the solution may have poor endurance. In order to guarantee stable, high-production yield, this might necessitate process tuning, which is unwelcome in logic e-NVM solutions. Overall, a combination of CHE programming and FN erasure seems the best option for e-NVM solutions with medium to high density.

		Type I	Type II	Type III
Scheme	Program	CHE	FN	CHE
	Erase	FN	FN	BBHH
Power	Program	~100uA/bit	<1nA/bit	~100uA/bit
	Erase	<1nA/bit	<1nA/bit	~1mA/bit
Time	Program	~100us	10ms–200ms	~100us
	Erase	5ms–200ms (per chip or sector)	5ms–200ms (per chip or sector)	2ms–5ms (per byte or word)
	Total (4Kb)	~0.05s	~5s	~1.8s
	Total (64Kb)	~0.8s	~163.8s	~16.38s
	Total (512Kb)	~6.5s	~640s	~135s
Memory Area		Good	Good for low density	Good
Reliability		Good	Good	Poor
Manufacturing Yield		Stable	Stable	Sensitive to process
Note: Calculate total testing time for full chip programming and chip erasure.				

Conclusion – As the leading logic e-NVM IP provider, eMemory offer two types of MTP solution to meet the e-NVM needs of various applications. One is NeoEE technology, which uses FN tunneling for both programming and erasure, and the other is NeoMTP technology, which uses CHE injection for programming and FN tunneling for erasure.

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About eMemory

eMemory is a global leader in logic process embedded non-volatile memory (eNVM) silicon IP established in 2000. eMemory has devoted itself to research and development of innovative technologies, offering the industry's most comprehensive platforms of patented eNVM IP solutions which are supplied to semiconductor foundries, integrated devices manufacturers (IDMs), and fabless design houses worldwide. eMemory's eNVM silicon IPs support a wide range of applications, including trimming, function selection, code storage, parameter setting, encryption, and identification setting. The company has the world's largest NVM engineering team and prides itself on providing partners with a full-service solution that sees the integration of eMemory eNVM IP from initial design stages through fabrication.

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